INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known	
Application Number	09/851,181
Filing Date	May-08, 2001
First Named Inventor	Theodore Valda
Group Art Unit	~~2155~~ 2661
Examiner Name	TRI H. PHAN
Attorney Docket No.	LSIL-01-035 / 01-035

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#3

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, caalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where	T
TP	1	A C Compiler for a Processor with a Reconfigurable Functional Unit; Proceedings of the 37th ACM/IEEE Conference on Design Automation Conference, 2000 - Author(s) - YE et al.	✓
TP	2	Using General-Purpose Programming Languages for FPGA Design; DAC 2000 - Author(s) - Hutchings et al.	✓
TP	3	Reconfigurable Computing: Its Concept and a Practical Embodiment Using Newly Developed Dynamically Reconfigurable Logic (DRL) LSI; ASP-DAC 2000 - Author(s) - Masakazu Yamashina	✓
TP	4	Reconfigurable Computing: What, Why and Implications for Design Automation; DAC 1999 - Author(s) - DeHorn et al.	✓
TP	5	An Automated Temporal Partitioning and Loop Fission Approach for FPGA Based Reconfigurable Synthesis of DSP Applications; DAC 1999 - Author(s) - Meenakshi Kaul	✓
TP	6	Dynamically Reconfigurable Architecture for Image Processor Applications; DAC 1999 - Author(s) - Alexandro Adario	✓
TP	7	A Representation for Dynamic Graphs in Reconfigurable Hardware and its Application to Fundamental Graph Algorithms; FPGA 2000 - Author(s) - Lorenz Huelsbergen	✓
TP	8	A Reconfigurable Multi-Function Computing Cache Architecture; DCNL Conference 2000 - Author(s) - Kim et al.	✓
TP	9	Communicating Logic: An Alternative Embedded Stream Processing Paradigm; ASP-DAC 2000 - Author(s) - Imlig et al.	✓
TP	10	The Application of Genetic Algorithms to the design of Reconfigurable Reasoning VLSI Chips; FPGA 2000 - Author(s) - Moritoshi Yasunaga	✓
TP	11	A Benchmark Suite for Evaluating Configurable Computing Systems - Status, Reflections, and Future Directions; FPGA 2000 - Author(s) - Kumar et al.	✓
TP	12	A Scheduling and Allocation Method to Reduce Data Transfer Time by Dynamic Reconfiguration; Asia and South Pacific DAC 2000 - Author(s) - Kazuhito Ito	✓
TP	13	An Architecture-Driven Metric for Simultaneous Placement and Global Routing for FPGA's ; DAC 2000 - Author(s) - Chang et al.	✓

Examiner signature		Date considered	1/15/05

PTO/SB/08A (10-96)
Approved for use thru[illegible]1/99. OMB 0651-0031
Patent and Trademark Office: U.S. DE[illegible]MENT OF COMMERCE

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TP	14	MorphoSys: Case Study of a Reconfigurable Computing System Targeting Multimedia Applications; DAC 2000 - Author(s) - Singh et al.	✓
TP	15	LSI Logic ASICs To Add Programmable-Logic Cores; http://www.eetimes.com/story/OEG19990729S0001; EE Times; July 29, 1999; 2 pages - Author(s) - MATSUMOTO	✓

Examiner signatur		Dat consid r d	1/15/05